I, the undersigned, who have prepared English translation which is attached herewith, hereby declare that the aforementioned translation is true and correct translation of officially certified copy of the Korean Patent Application No. 10-2003-30883 filed on May 15, 2003.

March 14, 2008

Translator : _____

Jin-Young KONG

[Specification]

[Title of the Invention]

TRANSISTOR HAVING MULTI CHANNEL AND METHOD OF FABRICATING THE SAME

[Brief Description of the Drawings]

Fig. 1A is a cross sectional view of a transistor according to the first embodiment of the present invention.

Fig. 1B is a cross sectional view taken along A-A of Fig. 1A.

Fig. 1C is a cross sectional view taken along B-B of Fig. 1C.

Fig. 1D is cross sectional view illustrating operation the transistor according to the first embodiment of the present invention.

Fig. 2A through Fig. 9A are cross-sectional views illustrating a method of fabricating the transistor according to the first embodiment of the present invention.

Fig. 2B through Fig. 9B are cross sectional views taken along A-A of Fig. 2A through Fig. 9A.

Fig. 2C through Fig. 9C are cross sectional views taken along B-B of Fig. 2A through Fig. 9A.

Fig. 10A is a cross sectional view of the transistor according to the second embodiment of the present invention.

Fig. 10B is a cross sectional view taken along A-A of Fig. 10A.

Fig. 10C is a cross sectional view taken along B-B of Fig. 10A.

[Detailed Description of the Invention]

[Object of the Invention]

[Field of the Invention and Prior Art related to the Invention]

The present invention relates to semiconductor devices and method of fabricating the same and, more specifically, to transistors and method of fabricating the same.

With reducing size of transistors and lowering driving voltage, output current is reduced. In addition, as channel length of transistors becomes short, short channel effect occurs and a leakage current is induced. Recently, all around transistor and silicon on insulator (SOI) transistor have been introduced to solve this problem.

[Technical Object of the Invention]

It is one feature of the present invention to provide transistors having high output current within limited dimensions and method of fabricating the same.

It is another feature of the present invention to provide transistors minimizing a leakage current and method of fabricating the same.

[Construction of the Invention]

Theses and other object of the present invention are accomplished through a transistor having multi-layered channel. The transistor is formed on a semiconductor substrate and includes a horizontal channel region comprising a plurality of channel layers isolated each other. A couple of vertical source/drain regions connected to the horizontal channel region are formed on both side of the horizontal channel region. A gate pattern intersects between a top surface of the horizontal channel region and each layer of the channel layers. A gate insulation layer is interposed between the horizontal channel region and the gate pattern. Source/drain electrodes are connected to vertical source/drain regions respectively.

A first insulation layer insulates the gate pattern and the source/drain electrodes from the semiconductor substrate. The lower most layer of the horizontal channel region is connected to the semiconductor substrate.

A mask pattern is further interposed between upper most of the horizontal channel region and the gate pattern. As a result, channels may not be formed on top of upper most of the horizontal channel region. Differently, the gate pattern can be extended between the mask pattern and an upper most channel layer because the mask pattern is vertically isolated to the upper most channel layer. At this time, channels are formed on top of the upper most channel layer. According to the present invention, the gate pattern can be formed by applying DAMASCEN process. Accordingly, the gate pattern may be formed in a second insulation layer covering a whole surface of the semiconductor substrate including the horizontal channel regions. That is, a second insulation layer has a gate opening crossing over top of the horizontal channel region. The gate opening is filled with the gate pattern. Also, the source/drain electrodes penetrate the second insulation layer to be connected to the source/drain regions.

Theses and other object of the present invention are accomplished by a method of fabricating the transistor having multi-layer channel. In this method, the trench is formed on the semiconductor substrate. At the same time, the first and second epitaxial patterns are alternately stacked to form a stacked structure on the region defined by the trench. A first insulation pattern is formed at bottom of the trench. A third epitaxial layer is grown on the surface of the first and second epitaxial patterns. A second insulation layer having a gate opening is formed on a whole surface of the semiconductor substrate. The gate opening exposes a part of the third epitaxial layer. A part of the first and second epitaxial patterns are exposed by removing the third epitaxial layer exposed in the gate opening. Horizontal channel regions of multi-layer isolated each other are formed by selectively isotropic etching the first epitaxial layers. A gate oxide layer is formed on surface of horizontal channel regions. A gate pattern is formed to fill gap regions of between horizontal channel regions. The gate pattern crosses over the horizontal channel regions. Source/drain electrodes, which penetrate the second insulation layer to be connected to the third epitaxial layer, are formed respectively on both side of the gate pattern.

Concretely, the stacked structure of the first and second epitaxial patterns are stacked can be formed by the following process.

The first and second epitaxial layers of multi-layer are stacked in rotation on the semiconductor substrate. Then, first and second epitaxial layers and the semiconductor substrate are sequentially patterned. Then, the trench is formed in a peripheral of the structure. The first epitaxial layer can be formed of silicon germanium layer, and the second epitaxial layer can be formed of silicon layer.

According to the present invention, a source/drain of a transistor can be formed by implanting impurities into the third epitaxial layer. A channel diffusion layer can be formed by implanting impurities into the second epitaxial layer.

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in different form and should not be construct as limited to the embodiments set forth herein. Rather these embodiments are provided so that this disclosure will be trough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to being "on" another layer or substrate, it can be directly on the other layer or substrate or intervening layers may be also be present. Like numbers refer to like elements throughout the specification.

Fig. 1A is a cross sectional view of a transistor according to the first embodiment of the present invention.

Fig. 1B is a cross sectional view taken along A-A of Fig. 1A.

Fig. 1C is a cross sectional view taken along B-B of Fig. 1C.

Referring to Fig. 1A, 1B and 1C, a transistor is formed on a region defined by a trench formed on a semiconductor substrate. The transistor includes horizontal channel regions of multi layer 14a and 50 and vertical source/drain regions 52. Horizontal channel regions 14a and 50 of multi layer are isolated each other. Vertical source/drain regions 52 are disposed on both side of horizontal channel regions 14a and 50. Horizontal channel

regions 14a and 50 comprise an active region 50 and epitaxial layers 14a. The active region 50 is defined by the trench 20, and epitaxial layers 14a are stacked sequentially on the semiconductor substrate. A gap region of horizontal channel regions 14a and 50 is filled with a gate pattern 34. The gate pattern crosses over the horizontal channel regions 14a and 50. A gate insulation layer 32 is interposed between horizontal channel regions 14a and 50 and the gate pattern 32. A mask pattern 16a is formed on top of upper most of horizontal channel regions 14a. The mask pattern 16a is interposed between upper most of horizontal channel regions 14a and the gate pattern 34. Vertical source/drain regions are connected to source/drain electrodes 42 respectively. A first insulation pattern 22 is interposed between source/drain electrodes 42 and the semiconductor substrate 10 to prevent leakage current path from the bottom of the source/drain electrode 42 to the semiconductor substrate. A whole surface of the semiconductor substrate including horizontal channel regions 14a and 50 and vertical source/drain regions 52 is covered with a second insulation layer 30. The gate pattern 34 can fill a gate opening formed at the second insulation layer 30 by applying DAMASCENE process. In addition, source/drain electrodes 42 penetrate the second insulation layer 30 to be connected to source/drain regions 52. A third insulation layer 36 can be further formed on the second insulation layer. In this case, the third insulation layer 36 electrically insulates an interconnection connected to source/drain electrodes 42 and the gate pattern 34. Additionally, an etch stop layer 26 can be further formed at bottom of the second insulation layer 30. The etch stop layer 26 prevents the first insulation pattern 22 from being etched excessively during forming source/drain electrodes 42. Also, the etch stop layer 26 prevents the first insulation pattern 22 from being etched excessively during forming the gate opening 28.

Fig. 1D is cross sectional view for illustrating operation the transistor according to a preferred embodiment of the present invention.

Referring to Fig. 1D, V_s and V_d are applied to a source 25s and a drain 52d, respectively. If V_g is applied to a gate electrode 34g, a channel (CH) is formed at the horizontal channel regions 14a and 50. In conventional transistor, one channel is formed when a gate voltage is applied. In gate all

around transistor, channels are formed on two sides or three sides of the substrate. On the other hand, in the transistor according to the present invention, driving current of the transistor can be increased regardless of occupation dimensions of the transistor because several channels are formed according to number of horizontal channel region stacked.

Fig. 2A through Fig. 9A are cross-sectional views for illustrating a method of fabricating the transistor according to the first embodiment of the present invention.

Fig. 2B through Fig. 9B are cross sectional views taken along A-A of Fig. 2A through Fig. 9A.

Fig. 2C through Fig. 9C are cross sectional views taken along B-B of Fig. 2A through Fig. 9A.

Referring to Fig. 2A, 2B and 2C, a stacked layer 18 is formed on the semiconductor substrate 10. A first epitaxial layer 12 and a second epitaxial layer 14 are alternately stacked to form the stacked layer 18. A number of layer of the first and second epitaxial layers 12 and 14 can be changeable. The first epitaxial layer 12 can be formed of a material (e.g., silicon germanium) having high etching rate in comparison with silicon composed of the semiconductor substrate. The second epitaxial layer 14 can be formed of same material as the semiconductor substrate (e.g., silicon). Upper most layer of the stacking layer 18 may be formed of the second epitaxial layer 14. A mask layer 14 can be further formed on the second epitaxial layer 14 of upper most layer 18.

The second epitaxial layer 14 can be doped by implanting impurities into the stacking layer 18 after forming the stacking structure 18 or during forming the first and second epitaxial layers 12 and 14.

Referring to Fig. 3A, 3B and 3C, the stacked layer 18 and the semiconductor substrate 10 are sequentially patterned to form a trench 20. The trench 20 defines an active region 50. At this time, a stacked pattern 18a is formed on the active region 50. The stacked pattern 18a is composed of first epitaxial layers 12a and second epitaxial layers 14a, which are alternately stacked on the active region 50. The stacking pattern can further include a mask pattern 16a.

Referring to Fig. 4A, AB and 4C, a first insulation pattern 22 is formed at bottom of the trench 20. The first insulation pattern 22 can be formed by forming an insulation layer on a whole surface of the semiconductor substrate and recessing the insulation layer. Consequently, the first insulation pattern 22 covers the substrate around the stacking pattern 18a. The first insulation pattern 22 can be formed by recessing the first insulation layer 22 until exposing the first epitaxial layer 12. As shown in Figs, surface of the active region can be disposed at low level than top of the first insulation pattern 22. Alternately, the surface of the active region can be disposed at high level than the top of the first insulation pattern 22.

Referring to Fig. 5A, 5B and 5C, selective epitaxial growth (SEG) process is applied to the semiconductor substrate to form a third epitaxial layer 24 on the surface of the stacked pattern 18a and exposed the surface of the semiconductor substrate. If the stacking pattern includes a mask pattern 16a, the third epitaxial layer 24 can be formed sidewalls of the stacking pattern 18a where the first and second epitaxial patterns 14a is exposed. The third epitaxial layer 24 can be formed of material having an etch selectivity with respect to the first epitaxial pattern 12a and the same material as the second epitaxial pattern 14a. For example, the third epitaxial layer 24 can be formed of silicon.

Source/drain regions can be formed by implanting impurities into the epitaxial layer 24. However, the source/drain regions can be formed in a subsequent process. The source/drain regions can be formed with conformal concentration using an oblique ion implantation.

Continuously, an etch stop layer 26 is formed on an whole surface of the semiconductor substrate 10. The reason for forming the etch stop layer is that excessive etching of the first insulation pattern 22 can be prevented. Accordingly, the etch stop layer 26 can be formed of a silicon nitride layer.

Referring to Fig. 6A, 6B and 6C, a second insulation layer 30 is formed on the whole surface of the semiconductor substrate. A gate opening 28 crossing over the stacking pattern 18a is formed by patterning the second insulation layer 30. In this case, the etch stop layer 26 is patterned continuously after patterning the second insulation layer 30. As a result, the

gate opening 28 exposes a part of the mask pattern 16, the third epitaxial layer 24 and the first insulation pattern 22.

Referring to Fig. 7A, 7B and 7C, the third epitaxial layer 24 in the gate opening 28 is removed to expose a part of the first epitaxial patterns 12a and the second epitaxial patterns 14a. Continuously, the first epitaxial layers 12 are etched using an isotropic etch process, thereby removing the first epitaxial layers 12 from the stacking pattern 18a. As a result, the second epitaxial layers 14 isolated at a predetermined space are disposed on the active region 50. Top of the active region 50 and the second epitaxial layers 14 are equivalent to a channel region of a transistor.

Continuously, a gate insulation layer 32 is formed on surface of the channel region. That is, the gate insulation layer 32 is formed on surface of the active region 50 and the second epitaxial layer 14. The gate insulation layer 32 can be formed conformally using thermal process or chemical vapor deposition method.

Referring to Fig. 8A, 8B and 8C, a gate pattern 34 filling the gate opening 28 is formed by applying DAMASCENE process. Specifically, a polysilicon layer is formed on a whole surface over the second insulation layer 30 with the gate opening 28. The polysilicon layer is planarized to form the gate pattern 34. Alternately, the polysilicon layer is formed in the gate opening 28 and a metal silicide layer is formed on the resultant structure which the polysilicon layer is formed. Then, the metal silicide layer is planarized to form the gate pattern 34. Consequently, the gate pattern 34 crosses over the stacked pattern 16a and filled in the gap region of between the channel regions. Therefore, the gate pattern 34 has a structure covering a plurality of the channel regions. Instead of forming the metal silicide layer, after forming a polysilicon gate pattern 34, a silicide layer can be formed by applying silicidation process on surface of the gate pattern 34 exposed. The channel of the transistor can be formed on surface of the second epitaxial patterns 14a and the active region opposite to the gate pattern 34.

Referring to Fig. 9A, 9B and 9C, a third insulation layer 36 is formed on an whole surface of the semiconductor substrate including the gate pattern 34. A source/drain contact hole 40 exposing the third epitaxial layer

24 is formed by sequentially patterning the third insulation layer 36 and the etch stop layer 26 at both side of the gate pattern 34. When the third epitaxial layer 24 is not doped, impurities can be implanted through the source/drain contact hole 40.

Different from substrate of typical plate MOS transistor, semiconductor substrate according to the present invention is not etched excessively during forming the source/drain contact hole 40 because the insulation layer is formed at bottom of the source/drain contact hole 40.

Continuously, a conductive layer is filled in the source/drain contact hole 40, so that a source/drain electrode 42 directly connected to the third epitaxial layer 24 is formed.

Fig. 10A is a cross sectional view of the transistor according to the second embodiment of the present invention.

Fig. 10B is a cross sectional view taken along A-A of Fig. 10A.

Fig. 10C is a cross sectional view taken along B-B of Fig. 10A.

Referring to Fig. 10A, 10B and 10C, the second embodiment of the present invention comprises a trench on a semiconductor substrate 10. Similar to the first embodiment, the transistor includes horizontal channel regions 14a and 50 and vertical source/drain regions 52. The horizontal channel regions 14a and 50 comprises a plurality of channel layers isolated each other, and the vertical source/drain regions 52 are in contact with both side of the horizontal channel regions 14a and 50. The horizontal channel regions 14a and 50 comprise an active region 50 and epitaxial layers 14a. The active region 50 is defined by the trench 20, and the epitaxial layers 14a are sequentially stacked on the semiconductor substrate. Different from the first embodiment, the upper most layer of the horizontal channel regions 14a and 50 are vertically isolated a mask pattern 16a. The gate pattern 34 is filled in a gap region of between the horizontal channel regions 14a, between upper most layer of the horizontal channel region and the mask pattern 16a. The gate pattern 34 crosses over the horizontal channel regions 14a and 50. The gate insulation layer 32 is interposed between the horizontal channel regions 14a and 50 and the gate pattern 34. Accordingly, different from the first embodiment, the channel can be formed top of upper most channel layer

of the horizontal channel regions. The method for forming the transistor according to the second embodiment is similar to the first embodiment. Contrary to the first embodiment, the upper most layer of the stacked layer (18 of Figs. 2A, 2B and 2C) is formed of a material having low etching rate in comparison with the semiconductor substrate. As a result, the upper most layer is removed to separate the mask pattern 16a from the horizontal channel region.

While the present invention has been described in detail by way of the embodiment thereof, it should be understood that the embodiment is not limitative of the invention. The spirit and the scope of the present invention are to be limited only by the appended claims.

[Effect of the Invention]

As previously mentioned, a two-layer epitaxial layer having an etch selectivity are repeatedly formed in rotation. A plurality of the horizontal channel regions can be stacked by removing any one of the two-layer epitaxial layer. Then, a plurality of channels are formed at the horizontal channel regions. High driving current can be obtained depending on number of layer of the horizontal channel regions. Therefore, without increasing occupation dimensions of the transistor, the transistor having high driving current can be formed. As a result, high-integrated devices are formed effectively.

Furthermore, the transistor includes the vertical source/drain region. Accordingly, the surface dimension of the source/drain regions is wide in spite of reducing junction depth of the source/drain regions. As a result, resistance can be reduced. In addition, leakage current can be dramatically reduced because the etching damages to the source/drain regions can be minimized in fabricating process.

[Scope of Claim]

1. A transistor comprising:

a horizontal channel region comprising a plurality of channels isolated from each other formed on a semiconductor substrate;

a couple of vertical source/drain regions formed on both side of the horizontal channel region respectively to be connected to the channels;

a gate pattern crossing over the horizontal channel region, and the gate pattern interposed between the channels;

a gate insulation layer interposed between the gate pattern and the horizontal channel region;

source/drain electrodes respectively connected to the vertical source/drain regions; and

a first insulation pattern interposed between each bottom of the source/drain region electrodes and the semiconductor substrate, the gate pattern and the semiconductor substrate, wherein the lower most layer of the horizontal channel regions is connected to the semiconductor substrate.

2. The transistor of claim 1, further comprising:

a mask pattern formed on the horizontal channel region to be directly connected to top of the upper most channel layer.

3. The transistor of claim 1, further comprising:

the mask pattern formed on the horizontal channel region, wherein the gate pattern is extended between the upper most channel layer and the mask pattern to cross over top of the upper most channel layer.

4. The transistor of claim 1, further comprising:

a second insulation pattern formed on whole semiconductor substrate including the horizontal channel region and the vertical source/drain regions; and

the second insulation layer has a gate opening intersecting top of the horizontal channel region,

wherein the gate pattern is formed in the gate opening, and

wherein the source/drain electrodes extended through the insulation pattern to be connected to the vertical source/drain regions

5. The transistor of claim 1, further comprising:

a third insulation layer formed on whole semiconductor substrate including the insulation pattern and the gate pattern,

wherein the source/drain electrodes extended through the third insulation layer and the second insulation pattern to be connected to the vertical source/drain regions.

6. The transistor of claim 1, wherein top of the first insulation pattern is positioned to high level as compared with the lowermost of the gate pattern.

7. A method of fabricating a transistor comprising the steps of:

forming a trench region to define an active region;

forming a stacking structure having first epitaxial patterns and second epitaxial patterns alternating on the active region;

forming a first insulation pattern on bottom of the trench;

growing a third epitaxial layer on the surface of the first, second epitaxial patterns;

forming a second insulation layer on a whole surface of the semiconductor substrate, the second insulation layer has a gate opening where the third epitaxial layer partially is exposed;

removing the third epitaxial layer in the gate opening to expose the first and second epitaxial patterns;

selectively isotropic etching the first epitaxial pattern to form a horizontal channel region having a plurality of channel layers isolated each other;

forming a gate oxide layer on the surface of channel layers;

forming a gate pattern crossing top of the horizontal channel and filling gap regions between channel layers and the gate opening; and

forming the source/drain electrodes penetrating the second insulation layer to be connected to the third epitaxial layer respectively on both sides of the gate pattern.

8. The method of fabricating the transistor of claim 7, wherein a step of forming the trench and a stacking structure comprises the steps of:

alternately stacking a plurality of the first and second epitaxial layers on the semiconductor substrate; and

patterning the first epitaxial layer, the second epitaxial layer and the semiconductor substrate to form a trench, and the first and second epitaxial patterns.

9. The method of fabricating the transistor of claim 8, wherein the first and third epitaxial layers are formed of silicon, and wherein the second epitaxial layer is formed of silicon germanium.

10. The method of fabricating the transistor of claim 7, wherein the upper surface of the first insulation pattern is formed lower than the lower most of the first epitaxial layer.

11. The method of fabricating the transistor of claim 7, prior to the step of forming the second insulation layer, further comprising:

forming an etch stop layer conformally on a resultant structure including the third epitaxial layer,

wherein the gate opening is formed by sequentially patterning the second insulation layer and the etch stop layer, and

wherein the source/drain electrodes penetrate the etch stop layer to be connected to the third epitaxial layer.

12. The method of fabricating the transistor of claim 7, prior to the step of forming the second insulation layer, further comprising:

implanting impurities in first and second epitaxial layers to form channel doped layers; and

implanting impurities into the third epitaxial layer to form source/drain regions.

13. The method of fabricating the transistor of claim 7, wherein the stacking structure of the first and second epitaxial patterns further comprises a mask pattern at the upper most layer, and

wherein the first and second epitaxial patterns are alternately stacked.

[Abstract of Disclosure]

[Abstract]

The present invention provides a transistor having multi-channel and method of fabricating the same. The transistor is formed on a semiconductor substrate and includes a plurality of horizontal channel regions isolated each other. A couple of vertical source/drain regions connected to the horizontal channel regions are formed on both sides of the horizontal channel regions. A gate pattern crosses over the horizontal channel region. A gate pattern is interposed between the horizontal channel regions. Source/drain electrodes are connected to the vertical source/drain regions, respectively. To form the horizontal channel region, a stacking structure having a plurality of the first and second epitaxial patterns in rotation is formed. Then, a third epitaxial layer is grown on the surface of the first and second epitaxial patterns. A second insulation layer having a gate opening, which partially exposes a third epitaxial layer on whole semiconductor substrate. The first and second epitaxial patterns partially exposed by removing the third epitaxial layer exposed. Continuously, the first epitaxial pattern is selectively isotropic etched. As a result, a plurality of the horizontal channel regions isolated each other can be formed.

[Representative Figure]

FIGs. 1A, 1B, 1C